## REMARKS

The enclosed is responsive to the Examiner's Office Action mailed on May 11, 2006. At the time the Examiner mailed the Office Action claims 1-28 were pending, and claims 11-17 were allowed. Applicant has made amended claims 1, 23, and 24. The Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

***Claim Rejections***

### 35 U.S.C. 102(b) Rejections

The Examiner rejected claims 1-9, 18-21, and 23-28 under 35 U.S.C. 102(b) as being anticipated by Osari, U.S. Patent No. 6,417,086 B1 (hereinafter "Osari").

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2131 of the MPEP recites: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

With respect to amended independent claim 1, Applicant teaches and claims: "A method comprising: forming a logic gate stack in a logic region on a substrate; forming a flash memory gate stack in a flash region on the substrate; depositing a hardmask layer over the logic gate stack and over the flash memory gate stack; patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired; patterning the flash gate stack in the flash region to form flash memory gates; and subsequently etching the logic gate stack using the remaining hardmask as a mask to form logic gates."

Osari discloses formation of EEPROM memory gates and logic gates. However, Osari does not disclose "patterning the flash gate stack in the flash region to form flash memory gates; and subsequently etching the logic gate stack using the remaining hardmask as a mask to form logic gates." Osari discloses the opposite. The logic gates of Osari are formed before the EEPROM gates are formed. See Col. 9, lines 9-25 and Figures 4I-4J. "In other words, in the CMOS logic circuit area, the single layer gates 51, 52 are formed by using the thin hard mask patterns 28Ad, 28Ac. Then, ... the CMOS logic circuit area is covered with a resist film. ... Finally, the double layer gates 53, 54, 55 are formed." Emphasis added.

Thus, Osari does not disclose "patterning the flash gate stack in the flash region to form flash memory gates; and subsequently etching the logic gate stack using the remaining hardmask as a mask to form logic gates," as required by claim 1.

Therefore, Osari does not set forth each and every element of claim 1. Pending independent claims 23 and 24 recite limitations that are similar to the limitations of claim 1, although some differences may exist among the limitations of the other pending independent claims. These similar limitations nevertheless patentably distinguish claims 23 and 24 over Osari. Therefore, for at least these reasons, Applicants respectfully submit that Osari does not anticipate all elements of independent claims 1, 23, and 24, and that these claims are in condition for allowance.

Claims 2-9 are dependent on independent claim 1. Claims 25-27 are dependent on independent claim 24. Thus, for at least the same reasons advanced above with respect to independent claims 1 and 24, Applicants respectfully submit that Osari does not anticipate all elements of dependent claims 2-9 and 25-27, and that these claims are in condition for allowance.

With respect to independent claim 18, Applicant teaches and claims: "An apparatus comprising: a substrate, the substrate having a logic region and a flash region; a logic gate stack formed on the substrate in the logic region, the logic gate stack having a top surface; regions of anti-reflective coating (ARC) formed on the top surface of the logic gate stack, the regions of ARC covering the areas of the logic gate stack where logic gates are to be formed; a plurality of flash memory gates formed on the substrate, the flash memory gates having a top surface; and a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack, and the top surface of the flash memory gates."

Osari does not disclose "a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack and the top surface of the flash memory gates."

Osari discloses a layer of resist in the following figures and corresponding text: Fig. 3G (Col. 8, lines 53-63), Fig. 4H (Col. 8, line 64 – Col. 9, line 4), Fig. 4J (Col. 9, lines 20-27), Fig. 7E (Col. 11, lines 10-18), Fig. 7G (Col. 11, lines 32-39), and Fig. 14G (Col. 3, lines 17-25). Each of these will be discussed in turn.

In Fig. 3G, Osari discloses a layer of resist (32d) formed in the logic circuit region. The resist covers the top surface of hardmask layer 28A. The top surface of the logic gate stack is not exposed, thus the resist does not cover the top surface of the gate stack. Furthermore, no regions of hardmask have been formed on the top surface of the gate stack; there is only a single layer of hardmask covering the entire top surface of the gate stack. Thus, the resist does not cover "the top surface of the logic gate stack," nor does it cover "the regions of ARC formed on top of the logic gate stack."

In Figs. 4H and 7E, Osari discloses a layer of resist (34b, 34c; 32d, 32e) formed in the logic circuit region. The resist covers the top surfaces of hardmask regions (28Ad, 28Ae; 30Bd, 30Be). However, the resist does not cover the top surface of the logic gate stack. The regions of resist are limited to covering the hardmask, because the resist was used to etch the hardmask. Thus, the resist does not cover "the top surface of the logic gate stack."

In Figs. 4J, 7G, and 14G Osari discloses a layer of resist (36; 34; 134) formed in the logic circuit region. The resist covers the already formed logic gates. Having already been etched away, the top surface of the logic gate stack is no longer exposed, thus the resist does not cover the top surface of the gate stack. The resist is limited to covering the hardmask formed on the top of each logic gate. Thus, the resist does not cover "the top surface of the logic gate stack."

Thus, although Osari does disclose a layer of resist, Osari does not disclose "a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack and the top surface of the flash memory gates." Therefore, Osari does not set forth each and every element of claim 18, and this claim is in condition for allowance.

Claims 19-21 are dependent on independent claim 18. Thus, for at least the same reasons advanced above with respect to independent claim 18, Applicants respectfully submit that Osari does not anticipate all elements of dependent claims 19-21, and that these claims are in condition for allowance.

## 35 U.S.C. 103(a) Rejections

The Examiner rejected claims 10, 22 and 28 under 35 U.S.C. 103(a) as being unpatentable over Osari, U.S. Patent No. 6,417,086 B1 (hereinafter "Osari").

In order to establish a prima facie case of obviousness: "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." In re Vaech, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, August 2001, §2143.

Claim 10 is dependent upon claim 1. Claim 22 is dependent upon claim 18. Claim 28 is dependent on claim 24. Thus, for at least the same reasons advanced above with respect to independent claims 1, 18, and 24, Osari does not teach or suggest all the claim limitations of dependent claims 10, 22, and 28 and these claims are in condition for allowance.

## Allowable Subject Matter

Applicant has noted, with appreciation, that the Examiner has allowed claims 11-17 over the prior art of record.

## CONCLUSION

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Cyndi M. Wheeler at (916) 356-5358.

If there are any charges, please charge Deposit Account No. 50-0221.

Respectfully Submitted,

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